WHAT IS CLAIMED IS:

1. A semiconductor device having a data inversion function in which data of a given cycle is compared with output data of a directly previous cycle to verify whether or not a majority in total bits constituting the data are switched and in which, when the majority number of bits of the data are switched, the data of said given cycle are inverted and the inverted data are output from a plurality of output terminals, said semiconductor device comprising:

a plurality of data comparator circuits, each being provided in associated one of a plurality of paths on which a plurality of data are transferred in parallel, with an output sequence from the output terminal between said plurality of data being predetermined, and comparing temporally before and after data;

a plurality of majority decision circuits, each receiving a plurality of comparison results which are output by the corresponding data comparator circuit, and the number of which corresponds to the number of said output terminals, and performing a majority decision of the comparison results received to output a decision result; and

a plurality of inversion flag generating circuits, each receiving the decision result from the corresponding majority decision circuit and generating an inversion flag indicating that data is inverted and is output from said output terminals, based on the decision result; wherein the decisions of data inversion for a plurality of cycles are made in parallel.

2. The semiconductor device according to claim 1, wherein one circuit group made up of said data comparator circuit, said majority decision

circuit and said inversion flag generating circuit are provided for a path on which data prescribed by a rising edge of double-rate clock signal is transferred and another circuit group made up of said data comparator circuit, said majority decision circuit and said inversion flag generating circuit are provided for a path on which data prescribed by a falling edge of the double-rate clock signal is transferred.

3. A semiconductor device comprising:

a plurality of data output terminals;

first to P-th ports for one of said output terminals, for outputting, in parallel, first to P-th bit data to be output via said one data output terminal, where P is a predetermined integer not less than two, said first to the P-th bit data being output in this order via each data output terminal;

first to P-th data comparator circuits provided in association with said first to P-th ports, an i-th data comparator circuit of said data comparator circuits, where i is an integer from 1 to P, comparing data of the (i-1)st port, where if i =1, (i-1)st port is the P-th port or an initial value, with data of the i-th port to output an i-th comparison flag signal,

first to P-th majority decision circuits provided in association with first to P-th data comparator circuits, the i-th majority decision circuit of said majority decision circuits, where i is an integer from 1 to P, receiving the i-th comparison signal, a number of which is equal to the number of the data output terminals of the semiconductor device and checking whether or not number of non-coincidence is the majority;

first to P-th inversion flag generating circuits provided in association with said majority decision circuits, the i-th inversion flag generating circuit of said first to P-th inversion flag generating circuits, where i is an integer from 1 to P, comparing an inversion flag signal of the (i-1)st one of said ports, where if i =1, (i-1)st port is the P-th port or an initial value, with the result of decision of the i-th majority decision circuit to output an i-th inversion flag signal; and

first to P-th data inversion circuits for controlling inversion of associated data based on the associated inversion flag signal, the i-th data inversion circuit of said data inversion circuits, where i is an integer from 1 to P, inverting data on said i-th port, thereby for the inverted data to be output from said data output terminal, if said i-th inversion flag signal indicates the inversion.

4. The semiconductor device according to claim 3, wherein the data of said first to P-th ports are sequenced, for said one data output terminal, in the order of the first port up to the P-th port, so that the data are serially converted and output.

5. A semiconductor device in which data are output twice from one data terminal during each clock cycle, based on a transition of the clock signal from a first logic value to a second logic value and a transition of the clock signal from said second logic value to said first logic value, said semiconductor device comprising:

first and second data comparator circuits, connected to first and second paths, respectively, the data output on a first transition of said clock signal from the first logic value to the second logic value and on a second transition thereof from the second logic value to the first logic value being transmitted on said first and second paths, respectively;

said first data comparator circuit verifying, by comparison, whether or not the data in a first transition timing of said clock signal on said first path is coincident with the data in a second transition timing of said clock signal directly previous to said first transition timing, on said second path to decide the presence or absence of data switching between said second transition directly previous to said first transition and said first transition and outputting the result of decision as a first output signal;

said second data comparator circuit verifying, by comparison, whether or not the data in the first transition timing of said clock signal on said first path is coincident with the data in the second transition timing of said clock signal next following said first transition timing, on said second path to decide the presence or absence of data switching between said first transition and the second transition next following to said first transition, and outputting the result of decision as a second output signal;

a first majority decision circuit, receiving a first group of output signals, which are output from said first data comparator circuit, and the number of which is equal to the data terminals of the semiconductor device, and verifying whether or not the majority of the data in said first group of the output signals have been switched to output a first decision result signal;

a second majority decision circuit, receiving a second group of output signals, which are output from said second data comparator circuits and the number of which is equal to the data output terminals of the semiconductor device, and verifying whether or not the majority of the data in said second group of the output signals have been switched to output a second decision result signal;

a first inversion flag generating circuit for generating a first inversion flag from said first decision result signal output from said first majority decision circuit and from the value of a second inversion flag previous at least by one transition of said clock signal;

a second inversion flag generating circuit for generating the second inversion flag from said second decision result signal from said second majority decision circuit and from the value of said first inversion flag previous at least by one transition of said clock signal;

a first data inversion circuit for inverting the data of said first path and outputting the resulting inverted data, if the first inversion flag indicates that the majority of the data have been switched; and

a second data inversion circuit for inverting the data of said second path and outputting the resulting inverted data if the first inversion flag indicates that the majority of the data have been switched;

wherein said first and second inversion flag generating circuits output said first and second inversion flag signals respectively, as flags indicating the inversion of the output data, from a control terminal of the semiconductor device.

6. The semiconductor device according to claim 5, wherein said first and second data comparator circuits and the first and second data inversion circuits are provided in a stage of a latch circuit unit provided on a data

bus on which data of said first and second paths are transferred to an output circuit.

7. The semiconductor device according to claim 5, further comprising:

a parallel-to-serial conversion circuit, receiving outputs from said first and second data inversion circuits in parallel, and performing parallel to serial conversion of said outputs to output the resulting serial data; and

an output buffer circuit receiving the output data from said parallel-to-serial conversion circuit to output the data from an output terminal.

8. The semiconductor device according to claim 6, wherein said latch circuit unit comprises:

first and second latch circuits connected to said first and second paths respectively, for sampling and outputting the first and second data, output to said first and second paths in parallel, with the first and second transitions of a first sampling clock signal, respectively;

a third latch circuit for sampling the output of said first latch circuit with one of the first and second transitions of the first sampling clock signal and for outputting the sampled signal with the other transition of the first sampling clock signal;

a fourth latch circuit, receiving an output of said second latch circuit, for sampling and outputting the signal with said one of the first and second transitions of said first sampling clock signal;

a fifth latch circuit, receiving an output of said fourth latch circuit, for sampling and outputting the signal with said one of the first and second transitions of said first sampling clock signal; and

a sixth latch circuit, receiving an output of said fifth latch circuit, for sampling and outputting the signal with the other of the first and second transitions of said first sampling clock signal.

9. The semiconductor device according to claim 8, wherein said first data inversion circuit comprises a first selection circuit receiving an output of said third latch circuit and an inverted signal thereof, and also receiving said first inversion flag signal, as a selection control signal, said first selection circuit outputting said inversion signal when said first inversion flag signal indicates inversion; and wherein

said second data inversion circuit comprises a second selection circuit receiving an output of said sixth latch circuit and an inverted signal thereof, and also receiving said second inversion flag signal, as a selection control signal, said second selection circuit outputting said inversion signal when said second inversion flag signal indicates inversion.

10. The semiconductor device according to claim 8, wherein said first data comparator circuit receives data of said first path and an output of said fourth latch circuit for detecting a coincidence thereof; and wherein said second data comparator circuit receives data of said first and second paths for detecting a coincidence thereof.

11. The semiconductor device according to claim 8, wherein said first inversion flag generating circuit includes a first comparator circuit for checking whether or not said first check result signal from said first majority decision circuit coincides with said second inversion flag from

said second inversion flag generating circuit; and

a seventh latch circuit for sampling an output of said first comparator circuit with one of the first and second transitions of a second sampling clock signal and outputting the output with the other transition of the second sampling clock signal; and wherein

said second inversion flag generating circuit includes an eighth latch circuit for sampling and outputting said second check result signal from said second majority decision circuit with the other of said first and second transitions of said second sampling clock signal;

a second comparator circuit for checking whether or not said first inversion flag from said first inversion flag generating circuit is coincident with an output of said eighth latch circuit; and

a ninth latch circuit for sampling an output of said eighth comparator circuit with one of the first and second transitions of said second sampling clock signal and for outputting the sampled output with the other transition of said second sampling clock signal.

12. The semiconductor device according to claim 8, further comprising means for resetting said fourth latch circuit.

13. The semiconductor device according to claim 11, further comprising means for resetting said ninth latch circuit.

14. The semiconductor device according to claim 11, wherein said first and second sampling clock signals are both generated by the clock signal supplied from outside the semiconductor device to the semiconductor device and are synchronized with each other.

15. The semiconductor device according to claim 11, further comprising

a clock synchronized type semiconductor memory for outputting read data from a cell array at a timing of a rising edge and a falling edge of a clock signal, wherein read data from the cell array of said semiconductor memories is output at a rising edge and at a falling edge of the clock signal.

16. A data inversion circuit for outputting parallel data composed by N bits, where N is an integer not less than two, said data inversion circuit comprising:

N sets of first to P-th data comparator means, in association with said N bits,

said first to P-th data comparator means classifying said parallel data into P sets of parallel data neighboring to one another in the outputting timing sequence, P being an integer not less than two, said first to P-th data comparator means comparing the logic value of each of the first to P-th parallel data with the logic value of the parallel data to be output temporally directly previously to said first to P-th parallel data, at the same bit positions as those of the first to P-th parallel data, and outputting a comparison result as a logic value indicating coincidence or non-coincidence;

first to P-th majority decision means, p-th majority decision means of said majority decision means, where p is an integer from not less than 1 to not larger than P, verifying whether or not the number of non-coincident ones of N logic values output from said P-th data comparator means of one of said N sets is larger than a preset number and outputting a decision result as a logic value;

first to P-th inversion flag generating means, p-th majority decision means of said inversion flag generating means, where p is an integer from not less than 1 to not larger than P, deciding whether or not there is a coincidence of an output logic value of the (p-1)st inversion flag with an output logic value of said p-th majority decision means, and outputting the logic value of the decision result as a p-th inversion flag;

data holding means holding output logic value of said P-th inversion flag generating means;

said first inversion flag generating means deciding whether or not there is a coincidence of an output logic value of said P-th inversion flag generating means, held by the data holding means, with an output logic value of said first majority decision means, and outputting the logic value of the decision result as a first inversion flag;

N sets of first to P-th data inversion means, in association with said N bits, said first to P-th data inversion means inverting the logic values in respective bit positions of said first to P-th parallel data responsive to said first to P-th inversion flags;

flag outputting means, receiving said first to P-th inversion flags in parallel output from said first to P-th inversion flag generating means and performing parallel to serial conversion of the inversion flags received to output serially the resultant inversion flag in a predetermined timing sequence; and

N sets of data outputting means, in association with said N bits, each data outputting means performing receiving output data signals in parallel from said first to P-th data inverting means and performing parallel to serial conversion of the signals received to output the resulting output data from the associated output terminal synchronized with the timing sequence of said inversion flags output by said flag outputting means.

17. A data inversion circuit according to claim 16, wherein at least one of said data comparator means, majority decision means, inversion flag generating means, data inverting means, flag outputting means and said data outputting means is operated in synchronization with a clock signal and wherein the inversion flag output from said flag outputting means is synchronized with said clock signal and data output from said data outputting means is synchronized with said clock signal.

18. The data inversion circuit according to claim 16, wherein at least one of said data comparator means, majority decision means, inversion flag generating means, data inverting means, flag outputting means and said data outputting means is operated in synchronization with rise and fall timings of a clock signal and wherein the inversion flag output from said flag outputting means is in synchronized with the rise and fall timings of said clock signal and data output from said flag outputting means is synchronized with the rise and fall timings of said clock signal.

19. The data inversion circuit as claimed in claim 16, wherein the inversion flag output from said flag outputting means includes the information as to whether or not the data output from said data outputting means is data obtained by inverting a logic value of the original data supplied to the data inversion circuit.

20. The data inversion circuit according to claim 16, wherein said P is 2

or 4.

21. The data inversion circuit according to claim 16, wherein said preset number is N/2 or an integer close up thereon.

22. A semiconductor device having a data inversion circuit as defined in claim 16.

23. A semiconductor device comprising:

a memory cell array; and

the data inversion circuit as defined in claim 16; wherein the P is equal to 2; and wherein a plural number of data read at a time by a pre-fetch operation from the memory cell array are separated into data associated with a rise of a clock signal and data associated with a fall of the clock signal and said data inversion circuit receiving the separated data.